ELEC 245 Introduction to Digital Systems
Spring 2014
Syllabus

General Information

Instructor:	Matthew Watkins	matthew.watkins@bucknell.edu
	Office: 332 Dana	Office Hours: See Moodle

Lectures: Monday, Wednesday, and Friday, 1:00-1:52pm, 366 Breakiron

Laboratory: Thursday 1:00-3:52 pm, 303 Dana

Class web page: `moodle.bucknell.edu`

Be sure to check that you are on the Moodle site. You should have received an email before the beginning of classes. If you did not receive a message, make sure you check that you are registered and that the course appears in Moodle.

You are encouraged to come to office hours to ask questions, get help with your homework or labs, or talk about careers and graduate school. Even if I am not officially holding office hours, I am available more often than not. If the door is open you are usually welcome, so try dropping in if you have a question. I will generally *not* be available on Tuesdays.

Description

Digital systems pervade our world and our lives. From television to cell phones to GPS to warfare to medicine to automobiles, computers and digital processing have reshaped the way we live and work. This course covers a broad spectrum of digital design, from single transistors and logic gates all the way up to complete microprocessors.

While most fields of engineering require extensive mathematics and complicated analysis for even rather simple components, digital systems merely require counting from 0 to 1. Their challenge, instead, is in combining many simple building blocks into a complex whole. This course will cover multiple layers of the computer design hierarchy that make designing these complex systems tractable.

Field programmable gate arrays (FPGAs), which today contain the equivalent of thousands or millions of logic gates, make it possible to build these complex systems in the lab without the tedium of manually connecting components. In this class, you will build complex digital systems and test them on a FPGA.

As you probably know, very few complex systems work the first time you put them together. Engineers must become good at systematically and efficiently debugging their creations. One of the course objectives that can be frustrating, but vitally important, is to learn to teach oneself how to debug systems using today's powerful but complex digital design tools.

Learning Objectives

At the end of the semester you should be able to:

- Analyze, design, and debug digital circuits (composed of both combinational and sequential logic) using schematics and Verilog (A)
- Optimize combinational logic circuits (A)

- Build a microprocessor in Verilog (A)
- Design and implement a finite state machine on an FPGA (A, B)

The parentheticals refer to ABET Student Outcomes.

Texts

"Digital Design and Computer Architecture," David M. Harris and Sarah L. Harris, Morgan Kaufmann Publishers, 2e, 2012.

Grading

Homework:	15%
Lab Assignments:	25%
Professionalism	5%
Midterm 1:	15%
Midterm 2:	15%
Final:	25%

Homework

- The course will include approximately weekly homework assignments.
- Unless otherwise specified on the homework assignment, homework must be submitted at the beginning of class on the day it is due.
- **No late homework** will be accepted. However, your lowest homework score will be dropped. Exceptions to this policy will **not** be granted except in *very* extenuating circumstances.
- Homework is to be completed individually and should be based on your individual abilities and understanding. You are, however, encouraged to study together and discuss information and concepts covered in lecture with other students.
- Make sure to cite any references, in print or on the Internet, which you use to aid in solving the homework.
- Please present your solutions in a clear and legible fashion. Solutions with an unnecessarily convoluted structure may receive less or no credit. Points may be deducted for sloppy submissions. In particular:
    - Make sure to write neatly and legibly.
    - Your name must be on the top of your solutions paper.
    - Your paper must be stapled.
    - Your solution must be chronological: problem 1 first, problem 2 second, and so forth.
    - Clearly state any assumptions you are making.
    - Make sure your final answer is clear by putting a box around it.

Lab Assignments

- There will generally be weekly lab assignments. Labs will typically be done in groups of two.
- In general, late labs **will not** be accepted. As a single exception, each student/group will be allowed *one* 24 hour extension for a single lab assignment. If it is a group assignment, then both students must have their extension available.
- Similar to homework, labs should be presented in a clear and legible fashion. Of particular note, material should be presented in the order requested.
- If you reference external materials, especially code, you must site the source.

Professionalism

- Out of respect to the professor and the other students in the class, you are expected to act professionally during all class activities. A non-exhaustive list of relevant items include:
  - Silencing cell phones and not texting in class,
  - Not using laptops or other technology during lecture without prior approval from the instructor,
  - Treating all students in the class professionally,
  - Participating in class discussions and activities, and
  - Arriving to class on time.

Midterms and Final – The course includes two midterms and a comprehensive final.

- Exams are closed book and closed notes.
- Calculators *may* be permitted. If they are permitted the calculator should be a simple scientific, non-programmable calculator. Laptops and cell phones will not be permitted as calculators.
- You are expected to present your exam solutions in a clear and legible fashion. Solutions with an unnecessarily convoluted structure may receive less or no credit.

Grade Distribution

A	93-100	C+	77-79
A-	90-92	C	73-76
B+	87-89	C-	70-72
B	83-86	D	60-69
B-	80-82	F	<60

The above grading scale *may* be relaxed at the end of the semester if I feel the scores do not accurately represent your progress. The opposite, however, will not occur.

Policies

Collaboration and External Resources – The work you submit in this course is expected to be the result of your individual effort, or in the case of lab assignments, the result of you and your partner's effort only. You are allowed and encouraged to study together and to discuss information and concepts covered in lecture with other students. At no point, however, should a student or group have a copy, in part or whole, of the work done by someone else. Work on exams must be entirely your own. Talking, collaboration, or copying from another student during an exam is not allowed.

You are allowed to reference external sources to aid in your completion of the homework and lab assignments so long as you appropriately site the source of the material. You may not, however, directly copy other's work or solutions.

Violation of any of these items will be reported to the Associate Dean of Engineering for submission to the Board of Review on Academic Responsibility. Please see the site on Academic Responsibility at Bucknell, www.bucknell.edu/x1324.xml, for more details.

Electronics Use – Please turn off cell phones during class. Laptops are not permitted during class except with the express prior approval of the instructor. Please see me outside of class if you wish to use a laptop or tablet during class.

Regrade Policy – Regrades of homework or lab assignments should be rare. For regrades of an assignment, return the assignment to the instructor within a week of the assignment being graded with a separate sheet of paper explaining the discrepancy. I will carefully regrade the entire assignment, read

the reasoning provided, and then make a final decision. Since the entire assignment is being regraded, it is possible the total score could go down as a consequence of previously undiscovered mistakes being found.

Bucknell University Honor Code
As a student and citizen of the Bucknell University community:

1. I will not lie, cheat or steal in my academic endeavors.
2. I will forthrightly oppose each and every instance of academic dishonesty.
3. I will let my conscience guide my decision to communicate directly with any person or persons I believe to have been dishonest in academic work.
4. I will let my conscience guide my decision on reporting breaches of academic integrity to the appropriate faculty or deans.

Bucknell University expectations for academic engagement
Courses at Bucknell that receive one unit of academic credit have a minimum expectation of 12 hours per week of student academic engagement. Student academic engagement includes both the hours of direct faculty instruction (or its equivalent) and the hours spent on out of class student work. Half and quarter unit courses at Bucknell should have proportionate expectations for student engagement.

Other Notes

- E-mail or in person is by far the best way to communicate with me. I check e-mail frequently and will do my best to respond promptly. Turnarounds, however, are not guaranteed to be fast.
- You are expected to check your e-mail and Moodle to keep abreast of any changes or announcements that may occur between classes.
- I reserve the right to modify or amend any portion of the course at any time to better support your learning. You will be given reasonable notification and explanation of any modification.